PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	Examiner: N t Yet Assigned
Name **Rene George et al**	Art Group: **1763**
Serial No. **10/665,267**	Att. Docket No.: **MAT-4**
Filed: **September 17, 2003**	Date: **December 27, 2003**
For: PHOTORESIST IMPLANT CRUST REMOVAL	

CERTIFICATE OF MAILING I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail in an envelope addressed to: Commissioner of Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on **December 27, 2003**.

Signed: _____
Jay R Beyer

Commissioner of Patents
P.O. Box 1450
Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT

Sir:

Enclosed is a copy of Information Disclosure Citation Form PTO-1449 together with copies of the documents cited on that form. It is respectfully requested that the cited documents be considered and that the enclosed copy of Information Disclosure Citation Form PTO-1449 be initialed by the Examiner to indicate such consideration and a copy thereof returned to applicant(s).

Pursuant to 37 C.F.R. § 1.97, the submission of this Information Disclosure Statement is not to be construed as a representation that a search has been made and is not to be construed as an admission that the information cited in this statement is material to patentability.

Pursuant to 37 C.F.R. § 1.97, this Information Disclosure Statement is being submitted under one of the following (as indicated by an "X" to the left of the appropriate paragraph):

__X__ 37 C.F.R. §1.97(b).

_____ 37 C.F.R. §1.97(c). If so, then enclosed with this Information Disclosure Statement is one of the following:

_____ A certification pursuant to 37 C.F.R. §1.97(e) or

_____ A check for $___ for the fee under 37 C.F.R. § 1.17(p).

_____ 37 C.F.R. §1.97(d). If so, then enclosed with this Information Disclosure Statement are the following:

(1) A certification pursuant to 37 C.F.R. §1.97(e);

(2) A petition requesting consideration of the Information Disclosure Statement; and

(3) Please charge Deposit Account No. **19-1685** (Order No. **MAT-4**) $___ for the fee under 37 C.F.R. §1.17(i) for submission of the Information Disclosure Statement. **(a duplicate copy of this sheet is enclosed)**

If there are any additional charges, please charge Deposit Account No. **19-1685** (Order No. **MAT-4**).

Respectfully submitted,

Jay R Beyer
Registration No. 39,907

Form 1449 (Modified)	Atty Docket No.	Serial No.:
	MAT-4	**10/665,267**
Information Disclosure	Applicants:	
Statement By Applicant	**Rene George et al**	
	Filing Date	Group
(Use Several Sheets if Necessary)	**9/17/03**	**1763**

U.S. Patent Documents

Examiner Initial	No.	Patent No.	Date	Patentee	Class	Sub-class	Filing Date
	A	US 6,524,936 B2	2/25/03	Hallock et al			
	B	US 6,342,446 B1	1/29/2003	Smith et al			
	C	US 6,426,304 B1	6/30/2002	Chien et al			
	D	US 6,379,576 B2	4/30/2002	Luo et al			
	E	US 6,352,936 B1	3/5/2002	Jehoul et al			
	F	US 6,342,446 B1	1/29/2002	Smith et al			
	G	US 6,277,733 B1	8/21/2001	Smith			
	H	US 6,251,771 B1	6/26/2001	Smith et al			
	I	5,628,871	5/13/1997	Shinagawa			
	J	5,534,231	7/9/1996	Savas			
	K	5,403,436	4/4/1995	Fujimura et al			
	L	4,980,022	12/25/1990	Fujimura et al			
	M	4,861,732	8/29/1989	Fujimura et al			
	N	4,861,424	8/29/1989	Fujimura et al			

Foreign Patent or Published Foreign Patent Application

Examiner Initial	No.	Document No.	Publication Date	Country or Patent Office	Class	Sub-class	Translation Yes	Translation No
	O							

Other Documents

Examiner Initial	No.	Author, Title, Date, Place (e.g. Journal) of Publication
	P	Boumerzoug et al, A Dry Process For Polymer Sidewall Residue Removal After Via-Hole Etching, 11/12/2000, 11th Annual IEEE/SEMI Advanced Semiconductor Manufacturing Conference and Workshop, Boston, MA (ASMC 2000)
	Q	Xu et al, Dry Cleaning Technologies For Post Metal And Via Applications, 7/13/1998, Symposium on Contamination Free Manufacturing for Semiconductor Processing, Semicon West 98, San Francisco, CA.
	R	Hu et al, Resist Stripping for Multilevel Interconnect Integrating Low k Dielectric Material, 2/2000, AVS First International Conference on Microelectronics and Interfaces.
	S	Gooch et al, Elimination Solvents From Semiconductor Wafer Manufacturing, 7/1/1999, 3rd Green Chemistry and Engineering Conference, Washington DC.
	T	Dopp et al, Manufacturing Qualifications of an All-Dry Via Deveil Plasma Process, 5/2000, 197th Electrochemical Society Meeting, Toronto, Canada.

Examiner	Date Considered

Examiner: Initial citation considered. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.